

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1406	body adj bias	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L2	53484	sram	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L3	246	1 and 2	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L4	1982	365/154.ccls.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L5	21	3 and 4	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L6	702	365/156.ccls.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L7	11	3 and 6	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L8	51	tang-stephen-h\$.in.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:13
L9	52	khellah-muhammad-m\$.in.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:14
L10	87	somasekhar-dinesh.in.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:14
L11	199	de-vivek-k\$.in.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:15
L12	51	tschanz-james-w\$.in.	US-PGPUB; USPAT	OR	ON	2006/08/11 17:15

Day : Friday  
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 **PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = KHELLAH

First Name = MUHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">10117163</a>	<a href="#">6724648</a>	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	KHELLAH, MUHAMMAD
<a href="#">10748222</a>	<a href="#">6903984</a>	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
<a href="#">10750566</a>	<a href="#">7001811</a>	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	KHELLAH, MUHAMMAD
<a href="#">11066395</a>	<a href="#">7031203</a>	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
<a href="#">10273627</a>	<a href="#">6801463</a>	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	KHELLAH, MUHAMMAD M.
<a href="#">10305753</a>	<a href="#">6909652</a>	150	11/26/2002	SRAM BIT-LINE REDUCTION	KHELLAH, MUHAMMAD M.
<a href="#">10330652</a>	Not Issued	89	12/27/2002	Multi-ported register files	KHELLAH, MUHAMMAD M.
<a href="#">10334410</a>	<a href="#">6784688</a>	150	12/30/2002	SKEWED REPEATER BUS	KHELLAH, MUHAMMAD M.
<a href="#">10334456</a>	<a href="#">6831871</a>	150	12/30/2002	STABLE MEMORY CELL READ	KHELLAH, MUHAMMAD M.
<a href="#">10334746</a>	Not Issued	30	12/31/2002	Method and apparatus for bus repeater tapering	KHELLAH, MUHAMMAD M.
<a href="#">10716755</a>	<a href="#">7072205</a>	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	KHELLAH, MUHAMMAD M.
<a href="#">10721184</a>	<a href="#">7002842</a>	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY	KHELLAH, MUHAMMAD M.

				WITH PURGE LINE	
<u>10738216</u>	<u>7020041</u>	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	KHELLAH, MUHAMMAD M.
<u>10738220</u>	<u>6876571</u>	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
<u>10740551</u>	<u>6952376</u>	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	KHELLAH, MUHAMMAD M.
<u>10746148</u>	<u>6906973</u>	150	12/24/2003	BITE-LINE DROOP REDUCTION	KHELLAH, MUHAMMAD M.
<u>10749734</u>	Not Issued	93	12/30/2003	1P1N 2T GAIN CELL	KHELLAH, MUHAMMAD M.
<u>10750572</u>	<u>6992339</u>	150	12/31/2003	ASYMMETRIC MEMORY CELL	KHELLAH, MUHAMMAD M.
<u>10810093</u>	<u>6985380</u>	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	KHELLAH, MUHAMMAD M.
<u>10812894</u>	Not Issued	71	03/31/2004	SRAM device having forward body bias control	KHELLAH, MUHAMMAD M.
<u>10813084</u>	<u>6992603</u>	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	KHELLAH, MUHAMMAD M.
<u>10879480</u>	<u>7098507</u>	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	KHELLAH, MUHAMMAD M.
<u>10880337</u>	Not Issued	95	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	KHELLAH, MUHAMMAD M.
<u>10880988</u>	Not Issued	41	06/30/2004	Interconnect structure in integrated circuits	KHELLAH, MUHAMMAD M.
<u>10881001</u>	Not Issued	93	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	KHELLAH, MUHAMMAD M.
<u>10942019</u>	Not Issued	30	09/16/2004	Charge storage memory cell	KHELLAH, MUHAMMAD M.
<u>10947765</u>	Not Issued	61	09/23/2004	Majority voter apparatus, systems, and methods	KHELLAH, MUHAMMAD M.

<a href="#">10954537</a>	Not Issued	95	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	KHELLAH, MUHAMMAD M.
<a href="#">10954931</a>	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	KHELLAH, MUHAMMAD M.
<a href="#">10956195</a>	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
<a href="#">10956285</a>	Not Issued	30	09/30/2004	Non volatile data storage through dielectric breakdown	KHELLAH, MUHAMMAD M.
<a href="#">10956407</a>	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	KHELLAH, MUHAMMAD M.
<a href="#">10979605</a>	Not Issued	95	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	KHELLAH, MUHAMMAD M.
<a href="#">11001870</a>	Not Issued	41	12/01/2004	Memory circuit	KHELLAH, MUHAMMAD M.
<a href="#">11008666</a>	Not Issued	71	02/22/2005	2-Transistor floating-body dram	KHELLAH, MUHAMMAD M.
<a href="#">11027476</a>	Not Issued	71	12/28/2004	One time programmable memory	KHELLAH, MUHAMMAD M.
<a href="#">11053786</a>	Not Issued	30	02/09/2005	Non strobe sensing circuit	KHELLAH, MUHAMMAD M.
<a href="#">11053788</a>	Not Issued	30	02/09/2005	Majority voter circuit design	KHELLAH, MUHAMMAD M.
<a href="#">11059174</a>	Not Issued	20	02/16/2005	Representative majority voter for bus invert coding	KHELLAH, MUHAMMAD M.
<a href="#">11134450</a>	Not Issued	30	05/23/2005	Reducing power consumption in integrated circuits	KHELLAH, MUHAMMAD M.
<a href="#">11137905</a>	Not Issued	30	05/25/2005	Memory with dynamically adjustable supply	KHELLAH, MUHAMMAD M.
<a href="#">11151982</a>	Not Issued	30	06/14/2005	Purge-based floating body memory	KHELLAH, MUHAMMAD M.
<a href="#">11158518</a>	Not Issued	30	06/21/2005	Apparatus and method for programming a memory array	KHELLAH, MUHAMMAD M.
<a href="#">11169106</a>	Not Issued	30	06/27/2005	Memory cell driver circuits	KHELLAH, MUHAMMAD M.
<a href="#">11170504</a>	Not Issued	30	06/29/2005	Capacitor structure for a logic process	KHELLAH, MUHAMMAD M.
<a href="#">11172078</a>	Not Issued	41	06/29/2005	Memory circuit	KHELLAH, MUHAMMAD M.
<a href="#">11172742</a>	Not Issued	30	06/30/2005	Operating an information storage cell array	KHELLAH, MUHAMMAD M.

<a href="#">11225912</a>	Not Issued	30	09/13/2005	Memory cell having p-type pass device	KHELLAH, MUHAMMAD M.
<a href="#">11239903</a>	Not Issued	30	09/30/2005	Dual gate oxide one time programmable (OTP) antifuse cell	KHELLAH, MUHAMMAD M.
<a href="#">11268098</a>	Not Issued	30	11/07/2005	Asymmetric memory cell	KHELLAH, MUHAMMAD M.

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**Search Another: Inventor**

Last Name	First Name
<input type="text" value="khellah"/>	<input type="text" value="muhammad"/>

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**PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR

First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08412183</a>	Not Issued	161	03/28/1995	APPARATUS AND METHOD FOR A REDUCED POWER MEMORY DIFFERENTIAL VOLTAGE SENSE-AMPLIFIER	SOMASEKHAR, DINESH
<a href="#">08937832</a>	<a href="#">6014041</a>	150	09/26/1997	DIFFERENTIAL CURRENT SWITCH LOGIC GATE	SOMASEKHAR, DINESH
<a href="#">08997071</a>	<a href="#">6002272</a>	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	SOMASEKHAR, DINESH
<a href="#">09539933</a>	<a href="#">6421289</a>	150	03/31/2000	METHOD AND APPARATUS FOR CHARGE-TRANSFER PRE-SENSING	SOMASEKHAR, DINESH
<a href="#">09690513</a>	<a href="#">6496402</a>	150	10/17/2000	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
<a href="#">09690687</a>	<a href="#">6421269</a>	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	SOMASEKHAR, DINESH
<a href="#">09733216</a>	<a href="#">6459316</a>	150	12/08/2000	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
<a href="#">09733482</a>	<a href="#">6701339</a>	150	12/08/2000	PIPELINED COMPRESSOR CIRCUIT	SOMASEKHAR, DINESH
<a href="#">09740104</a>	<a href="#">6351156</a>	150	12/18/2000	Noise reduction circuit	SOMASEKHAR, DINESH
<a href="#">09796072</a>	<a href="#">6982589</a>	150	02/28/2001	MULTI-STAGE MULTIPLEXER	SOMASEKHAR, DINESH
<a href="#">09823575</a>	<a href="#">6608786</a>	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
<a href="#">09873557</a>	<a href="#">7080111</a>	150	06/04/2001	FLOATING POINT MULTIPLY ACCUMULATOR	SOMASEKHAR, DINESH

<u>09873721</u>	<u>6889241</u>	150	06/04/2001	FLOATING POINT ADDER	SOMASEKHAR, DINESH
<u>09941053</u>	<u>6567329</u>	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND ACCESSOR	SOMASEKHAR, DINESH
<u>09966586</u>	<u>6757784</u>	150	09/28/2001	HIDING REFRESH OF MEMORY AND REFRESH- HIDDEN MEMORY	SOMASEKHAR, DINESH
<u>10117163</u>	<u>6724648</u>	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	SOMASEKHAR, DINESH
<u>10208130</u>	<u>6597223</u>	150	07/30/2002	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
<u>10241791</u>	<u>6707708</u>	150	09/10/2002	STATIC RANDOM ACCESS MEMORY WITH SYMMETRIC LEAKAGE- COMPENSATED BIT LINE	SOMASEKHAR, DINESH
<u>10267951</u>	<u>6784722</u>	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	SOMASEKHAR, DINESH
<u>10273627</u>	<u>6801463</u>	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	SOMASEKHAR, DINESH
<u>10300398</u>	<u>6721222</u>	150	11/19/2002	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
<u>10305753</u>	<u>6909652</u>	150	11/26/2002	SRAM BIT-LINE REDUCTION	SOMASEKHAR, DINESH
<u>10316728</u>	<u>6707755</u>	150	12/11/2002	HIGH VOLTAGE DRIVER	SOMASEKHAR, DINESH
<u>10324177</u>	<u>6879531</u>	150	12/19/2002	REDUCED READ DELAY FOR SINGLE-ENDED SENSING	SOMASEKHAR, DINESH
<u>10324178</u>	<u>6724649</u>	150	12/19/2002	MEMORY CELL LEAKAGE REDUCTION	SOMASEKHAR, DINESH
<u>10334456</u>	<u>6831871</u>	150	12/30/2002	STABLE MEMORY CELL READ	SOMASEKHAR, DINESH
<u>10461293</u>	<u>6801465</u>	150	06/13/2003	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
<u>10691342</u>	Not	41	10/21/2003	Hiding refresh of memory and	SOMASEKHAR,

	Issued			refresh-hidden memory	DINESH
<u>10716755</u>	<u>7072205</u>	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	SOMASEKHAR, DINESH
<u>10721178</u>	Not Issued	61	11/26/2003	Systolic memory arrays	SOMASEKHAR, DINESH
<u>10721184</u>	<u>7002842</u>	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
<u>10738216</u>	<u>7020041</u>	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	SOMASEKHAR, DINESH
<u>10738220</u>	<u>6876571</u>	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	SOMASEKHAR, DINESH
<u>10740551</u>	<u>6952376</u>	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	SOMASEKHAR, DINESH
<u>10746148</u>	<u>6906973</u>	150	12/24/2003	BITE-LINE DROOP REDUCTION	SOMASEKHAR, DINESH
<u>10748222</u>	<u>6903984</u>	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
<u>10749734</u>	Not Issued	93	12/30/2003	1P1N 2T GAIN CELL	SOMASEKHAR, DINESH
<u>10750566</u>	<u>7001811</u>	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	SOMASEKHAR, DINESH
<u>10750572</u>	<u>6992339</u>	150	12/31/2003	ASYMMETRIC MEMORY CELL	SOMASEKHAR, DINESH
<u>10810093</u>	<u>6985380</u>	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	SOMASEKHAR, DINESH
<u>10812894</u>	Not Issued	71	03/31/2004	SRAM device having forward body bias control	SOMASEKHAR, DINESH
<u>10879480</u>	<u>7098507</u>	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	SOMASEKHAR, DINESH



<a href="#">10880337</a>	Not Issued	95	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
<a href="#">10881001</a>	Not Issued	93	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
<a href="#">10942019</a>	Not Issued	30	09/16/2004	Charge storage memory cell	SOMASEKHAR, DINESH
<a href="#">10947869</a>	Not Issued	95	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	SOMASEKHAR, DINESH
<a href="#">10954537</a>	Not Issued	95	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	SOMASEKHAR, DINESH
<a href="#">10954931</a>	<a href="#">7061806</a>	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	SOMASEKHAR, DINESH
<a href="#">10956195</a>	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	SOMASEKHAR, DINESH
<a href="#">10956285</a>	Not Issued	30	09/30/2004	Non volatile data storage through dielectric breakdown	SOMASEKHAR, DINESH

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**PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = DE

First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08997071</a>	<a href="#">6002272</a>	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	DE, VIVEK
<a href="#">09001449</a>	<a href="#">5986473</a>	150	12/31/1997	DIFFERENTIAL, MIXED SWING, TRISTATE DRIVER CIRCUIT FOR HIGH PERFORMANCE AND LOW POWER ON-CHIP INTERCONNECTS	DE, VIVEK
<a href="#">10117163</a>	<a href="#">6724648</a>	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	DE, VIVEK
<a href="#">10273627</a>	<a href="#">6801463</a>	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	DE, VIVEK
<a href="#">10330652</a>	Not Issued	89	12/27/2002	Multi-ported register files	DE, VIVEK
<a href="#">10748222</a>	<a href="#">6903984</a>	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
<a href="#">10748298</a>	<a href="#">7030676</a>	150	12/31/2003	TIMING CIRCUIT FOR SEPARATE POSITIVE AND NEGATIVE EDGE PLACEMENT IN A SWITCHING DC-DC CONVERTER	DE, VIVEK
<a href="#">10919672</a>	Not Issued	25	08/16/2004	Stepwise drivers for DC/DC converters	DE, VIVEK
<a href="#">10924482</a>	Not Issued	61	08/23/2004	DC/DC converters using dynamically-adjusted variable-size switches	DE, VIVEK

<u>10954464</u>	Not Issued	30	09/30/2004	CPU power delivery system	DE, VIVEK
<u>10987278</u>	Not Issued	61	11/12/2004	Level shifter	DE, VIVEK
<u>11066395</u>	<u>7031203</u>	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
<u>11111060</u>	Not Issued	30	04/21/2005	Level shifter	DE, VIVEK
<u>11167978</u>	Not Issued	41	06/27/2005	Voltage regulation using digital voltage control	DE, VIVEK
<u>11170559</u>	Not Issued	30	06/28/2005	Low-voltage, buffered bandgap reference with selectable output voltage	DE, VIVEK
<u>11173065</u>	Not Issued	30	06/30/2005	Multiphase transformer for a multiphase DC-DC converter	DE, VIVEK
<u>11173760</u>	Not Issued	25	06/30/2005	DC-DC converter switching transistor current measurement technique	DE, VIVEK
<u>11323675</u>	Not Issued	20	12/30/2005	Error-detection flip-flop	DE, VIVEK
<u>09218723</u>	<u>6154045</u>	150	12/22/1998	METHOD AND APPARATUS FOR REDUCING SIGNAL TRANSMISSION DELAY USING SKEWED GATES	DE, VIVEK K
<u>09470275</u>	<u>6518833</u>	150	12/22/1999	LOW VOLTAGE PVT INSENSITIVE MOSFET BASED VOLTAGE REFERENCE CIRCUIT	DE, VIVEK K.
<u>09505212</u>	Not Issued	161	02/16/2000	Forward body biased transistors with reduced temperature	DE, VIVEK K.
<u>09527344</u>	<u>6492837</u>	150	03/17/2000	DOMINO LOGIC WITH OUTPUT PREDISCHARGE	DE, VIVEK K.
<u>09537971</u>	<u>6359802</u>	150	03/28/2000	One-transistor and one-capacitor dram cell for logic process technology	DE, VIVEK K.
<u>09540230</u>	Not Issued	161	03/31/2000	Footless domino gate	DE, VIVEK K.
<u>09607495</u>	<u>6518796</u>	150	06/30/2000	DYNAMIC CMOS CIRCUITS WITH INDIVIDUALLY ADJUSTABLE NOISE IMMUNITY	DE, VIVEK K.
<u>09608314</u>	<u>6429711</u>	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE	DE, VIVEK K.

				PRE-CHARGE AND STACK NODE PRE-DISCHARGE	
<u>09608457</u>	<u>6552887</u>	150	06/29/2000	VOLTAGE DEPENDENT CAPACITOR CONFIGURATION FOR HIGHER SOFT ERROR RATE TOLERANCE	DE, VIVEK K.
<u>09672689</u>	<u>6683467</u>	150	09/29/2000	METHOD AND APPARATUS FOR PROVIDING ROTATIONAL BURN-IN STRESS TESTING	DE, VIVEK K.
<u>09672695</u>	<u>6459293</u>	150	09/29/2000	MULTIPLE PARAMETER TESTING WITH IMPROVED SENSITIVITY	DE, VIVEK K.
<u>09672696</u>	<u>6632686</u>	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	DE, VIVEK K.
<u>09675579</u>	<u>6519176</u>	150	09/29/2000	DUAL THRESHOLD SRAM CELL FOR SINGLE-ENDED SENSING	DE, VIVEK K.
<u>09677698</u>	<u>6849909</u>	150	09/28/2000	METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR	DE, VIVEK K.
<u>09690687</u>	<u>6421269</u>	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	DE, VIVEK K.
<u>09707528</u>	<u>6744301</u>	150	11/07/2000	SYSTEM USING BODY- BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALTIES AND NOISE	DE, VIVEK K.
<u>09727025</u>	Not Issued	161	11/30/2000	Reference voltage translation circuit	DE, VIVEK K.
<u>09727173</u>	<u>6346803</u>	150	11/30/2000	Current reference	DE, VIVEK K.
<u>09727176</u>	<u>6433624</u>	150	11/30/2000	THRESHOLD VOLTAGE GENERATION CIRCUIT	DE, VIVEK K.
<u>09731515</u>	<u>6486706</u>	150	12/06/2000	DOMINO LOGIC WITH LOW- THRESHOLD NMOS PULL-UP	DE, VIVEK K.
<u>09740104</u>	<u>6351156</u>	150	12/18/2000	Noise reduction circuit	DE, VIVEK K.

<a href="#">09820067</a>	<a href="#">6429726</a>	150	03/27/2001	ROBUST FORWARD BODY BIAS GENERATION CIRCUIT WITH DIGITAL TRIMMING FOR DC POWER SUPPLY VARIATION	DE, VIVEK K.
<a href="#">09820579</a>	<a href="#">6608513</a>	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	DE, VIVEK K.
<a href="#">09821531</a>	<a href="#">6469572</a>	150	03/28/2001	FORWARD BODY BIAS GENERATION CIRCUITS BASED ON DIODE CLAMPS	DE, VIVEK K.
<a href="#">09823575</a>	<a href="#">6608786</a>	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	DE, VIVEK K.
<a href="#">09823633</a>	<a href="#">6496040</a>	150	03/30/2001	TRADING OFF GATE DELAY VERSUS LEAKAGE CURRENT USING DEVICE STACK EFFECT	DE, VIVEK K.
<a href="#">09846514</a>	Not Issued	161	04/30/2001	CMOS bus pulsing	DE, VIVEK K.
<a href="#">09846604</a>	<a href="#">6515513</a>	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	DE, VIVEK K.
<a href="#">09855910</a>	<a href="#">6445216</a>	150	05/14/2001	SENSE AMPLIFIER HAVING REDUCED VT MISMATCH IN INPUT MATCHED DIFFERENTIAL PAIR	DE, VIVEK K.
<a href="#">09894464</a>	<a href="#">6518817</a>	150	06/28/2001	VOLTAGE BUFFER	DE, VIVEK K.
<a href="#">09894465</a>	<a href="#">6763484</a>	150	06/28/2001	BODY BIAS USING SCAN CHAINS	DE, VIVEK K.
<a href="#">09941053</a>	<a href="#">6567329</a>	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND ACCESSOR	DE, VIVEK K.

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**PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = TSCHANZ

First Name = JAMES

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">10956195</a>	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TSCHANZ, JAMES
<a href="#">11323675</a>	Not Issued	20	12/30/2005	Error-detection flip-flop	TSCHANZ, JAMES
<a href="#">09608314</a>	<a href="#">6429711</a>	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE-DISCHARGE	TSCHANZ, JAMES W.
<a href="#">09672696</a>	<a href="#">6632686</a>	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	TSCHANZ, JAMES W.
<a href="#">09707528</a>	<a href="#">6744301</a>	150	11/07/2000	SYSTEM USING BODY-BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALTIES AND NOISE	TSCHANZ, JAMES W.
<a href="#">09820579</a>	<a href="#">6608513</a>	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	TSCHANZ, JAMES W.
<a href="#">09846514</a>	Not Issued	161	04/30/2001	CMOS bus pulsing	TSCHANZ, JAMES W.
<a href="#">09846604</a>	<a href="#">6515513</a>	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	TSCHANZ, JAMES W.
<a href="#">09894465</a>	<a href="#">6763484</a>	150	06/28/2001	BODY BIAS USING SCAN CHAINS	TSCHANZ, JAMES W.
<a href="#">10010046</a>	<a href="#">6642765</a>	150	12/06/2001	TRANSMISSION-GATE BASED FLIP-FLOP	TSCHANZ, JAMES W.
<a href="#">10267951</a>	<a href="#">6784722</a>	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY	TSCHANZ, JAMES W.

				BIAS GRID	
<u>10328573</u>	Not Issued	93	12/23/2002	METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION THROUGH DYNAMIC CONTROL OF SUPPLY VOLTAGE AND BODY BIAS INCLUDING MAINTAINING A SUBSTANTIALLY CONSTANT OPERATING FREQUENCY	TSCHANZ, JAMES W.
<u>10330544</u>	<u>6806739</u>	150	12/30/2002	TIME-BORROWING N-ONLY CLOCKED CYCLE LATCH	TSCHANZ, JAMES W.
<u>10334410</u>	<u>6784688</u>	150	12/30/2002	SKEWED REPEATER BUS	TSCHANZ, JAMES W.
<u>10334746</u>	Not Issued	30	12/31/2002	Method and apparatus for bus repeater tapering	TSCHANZ, JAMES W.
<u>10673283</u>	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TSCHANZ, JAMES W.
<u>10703562</u>	<u>7096433</u>	150	11/10/2003	METHOD FOR POWER CONSUMPTION REDUCTION	TSCHANZ, JAMES W.
<u>10738216</u>	<u>7020041</u>	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TSCHANZ, JAMES W.
<u>10745029</u>	<u>7015741</u>	150	12/23/2003	ADAPTIVE BODY BIAS FOR CLOCK SKEW COMPENSATION	TSCHANZ, JAMES W.
<u>10746759</u>	<u>7051295</u>	150	12/23/2003	IC DESIGN PROCESS INCLUDING AUTOMATED REMOVAL OF BODY CONTACTS FROM MOSFET DEVICES	TSCHANZ, JAMES W.
<u>10747805</u>	<u>7075180</u>	150	12/29/2003	METHOD AND APPARATUS FOR APPLYING BODY BIAS TO INTEGRATED CIRCUIT DIE	TSCHANZ, JAMES W.
<u>10792262</u>	<u>6917237</u>	150	03/02/2004	TEMPERATURE DEPENDENT REGULATION OF THRESHOLD VOLTAGE	TSCHANZ, JAMES W.
<u>10812894</u>	Not Issued	71	03/31/2004	SRAM device having forward body bias control	TSCHANZ, JAMES W.
<u>10813084</u>	<u>6992603</u>	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	TSCHANZ, JAMES W.
<u>10873243</u>	<u>6970018</u>	150	06/23/2004	CLOCKED CYCLE LATCH	TSCHANZ, JAMES

				CIRCUIT	W.
<u>10879486</u>	Not Issued	30	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TSCHANZ, JAMES W.
<u>10880988</u>	Not Issued	41	06/30/2004	Interconnect structure in integrated circuits	TSCHANZ, JAMES W.
<u>10947765</u>	Not Issued	61	09/23/2004	Majority voter apparatus, systems, and methods	TSCHANZ, JAMES W.
<u>10947869</u>	Not Issued	95	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	TSCHANZ, JAMES W.
<u>10953199</u>	Not Issued	61	09/28/2004	Frequency management apparatus, systems, and methods	TSCHANZ, JAMES W.
<u>10953865</u>	Not Issued	83	09/30/2004	System and method for applying within-die adaptive body bias	TSCHANZ, JAMES W.
<u>10954256</u>	Not Issued	40	09/29/2004	Control circuitry in stacked silicon	TSCHANZ, JAMES W.
<u>10955383</u>	Not Issued	30	09/30/2004	Power management integrated circuit	TSCHANZ, JAMES W.
<u>10982266</u>	Not Issued	95	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	TSCHANZ, JAMES W.
<u>11018011</u>	Not Issued	41	12/20/2004	Body biasing for dynamic circuit	TSCHANZ, JAMES W.
<u>11018016</u>	Not Issued	25	12/20/2004	Body biasing methods and circuits	TSCHANZ, JAMES W.
<u>11038134</u>	Not Issued	41	01/21/2005	Bias generator for body bias	TSCHANZ, JAMES W.
<u>11038394</u>	Not Issued	71	01/21/2005	Bias generator for body bias	TSCHANZ, JAMES W.
<u>11053788</u>	Not Issued	30	02/09/2005	Majority voter circuit design	TSCHANZ, JAMES W.
<u>11059174</u>	Not Issued	20	02/16/2005	Representative majority voter for bus invert coding	TSCHANZ, JAMES W.
<u>11094574</u>	Not Issued	30	03/31/2005	Method and apparatus to adjust die frequency	TSCHANZ, JAMES W.
<u>11134450</u>	Not Issued	30	05/23/2005	Reducing power consumption in integrated circuits	TSCHANZ, JAMES W.
<u>11295400</u>	Not Issued	30	12/06/2005	Component reliability budgeting system	TSCHANZ, JAMES W.
<u>11314236</u>	Not Issued	25	12/22/2005	Single-stage and multi-stage low power interconnect architectures	TSCHANZ, JAMES W.



<a href="#">11320789</a>	Not Issued	30	12/30/2005	Method and apparatus to clamp SRAM supply voltage	TSCHANZ, JAMES W.
<a href="#">11321100</a>	Not Issued	20	12/29/2005	Reliability degradation compensation using body bias	TSCHANZ, JAMES W.
<a href="#">11324628</a>	Not Issued	20	01/03/2006	Bidirectional body bias regulation	TSCHANZ, JAMES W.
<a href="#">11486030</a>	Not Issued	20	07/14/2006	Method and apparatus for power consumption reduction	TSCHANZ, JAMES W.

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**PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = TANG

First Name = STEPHEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">10748222</a>	<a href="#">6903984</a>	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
<a href="#">10987278</a>	Not Issued	61	11/12/2004	Level shifter	TANG, STEPHEN
<a href="#">11066395</a>	<a href="#">7031203</a>	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
<a href="#">11111060</a>	Not Issued	30	04/21/2005	Level shifter	TANG, STEPHEN
<a href="#">10014009</a>	Not Issued	161	12/10/2001	BALANCING GATE-LEAKAGE CURRENT IN DIFFERENTIAL PAIR CIRCUITS	TANG, STEPHEN H.
<a href="#">10025047</a>	<a href="#">6693332</a>	150	12/19/2001	CURRENT REFERENCE APPARATUS	TANG, STEPHEN H.
<a href="#">10162929</a>	<a href="#">6643199</a>	150	06/04/2002	MEMORY WITH REDUCED SUB-THRESHOLD LEAKAGE CURRENT IN DYNAMIC BIT LINES OF READ PORTS	TANG, STEPHEN H.
<a href="#">10267951</a>	<a href="#">6784722</a>	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	TANG, STEPHEN H.
<a href="#">10330652</a>	Not Issued	89	12/27/2002	Multi-ported register files	TANG, STEPHEN H.
<a href="#">10334644</a>	<a href="#">6710642</a>	150	12/30/2002	BIAS GENERATION CIRCUIT	TANG, STEPHEN H.
<a href="#">10673283</a>	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TANG, STEPHEN H.
<a href="#">10689128</a>	<a href="#">6975005</a>	150	10/20/2003	CURRENT REFERENCE APPARATUS AND SYSTEMS	TANG, STEPHEN H.

<u>10716755</u>	<u>7072205</u>	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	TANG, STEPHEN H.
<u>10721184</u>	<u>7002842</u>	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
<u>10738216</u>	<u>7020041</u>	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TANG, STEPHEN H.
<u>10740551</u>	<u>6952376</u>	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	TANG, STEPHEN H.
<u>10746148</u>	<u>6906973</u>	150	12/24/2003	BITE-LINE DROOP REDUCTION	TANG, STEPHEN H.
<u>10747084</u>	<u>6870418</u>	150	12/30/2003	TEMPERATURE AND/OR PROCESS INDEPENDENT CURRENT GENERATION CIRCUIT	TANG, STEPHEN H.
<u>10749734</u>	Not Issued	93	12/30/2003	1P1N 2T GAIN CELL	TANG, STEPHEN H.
<u>10750566</u>	<u>7001811</u>	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	TANG, STEPHEN H.
<u>10750572</u>	<u>6992339</u>	150	12/31/2003	ASYMMETRIC MEMORY CELL	TANG, STEPHEN H.
<u>10812894</u>	Not Issued	71	03/31/2004	SRAM device having forward body bias control	TANG, STEPHEN H.
<u>10879480</u>	<u>7098507</u>	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	TANG, STEPHEN H.
<u>10879486</u>	Not Issued	30	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TANG, STEPHEN H.
<u>10880337</u>	Not Issued	95	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	TANG, STEPHEN H.
<u>10881001</u>	Not Issued	93	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	TANG, STEPHEN H.
<u>10942019</u>	Not Issued	30	09/16/2004	Charge storage memory cell	TANG, STEPHEN H.
<u>10953865</u>	Not	83	09/30/2004	System and method for applying	TANG, STEPHEN

	Issued			within-die adaptive body bias	H.
<a href="#">10954537</a>	Not Issued	95	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	TANG, STEPHEN H.
<a href="#">10954931</a>	<a href="#">7061806</a>	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	TANG, STEPHEN H.
<a href="#">10956195</a>	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TANG, STEPHEN H.
<a href="#">10956285</a>	Not Issued	30	09/30/2004	Non volatile data storage through dielectric breakdown	TANG, STEPHEN H.
<a href="#">10956407</a>	<a href="#">7075821</a>	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	TANG, STEPHEN H.
<a href="#">10979605</a>	Not Issued	95	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	TANG, STEPHEN H.
<a href="#">10982266</a>	Not Issued	95	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	TANG, STEPHEN H.
<a href="#">11008666</a>	Not Issued	71	02/22/2005	2-Transistor floating-body dram	TANG, STEPHEN H.
<a href="#">11027476</a>	Not Issued	71	12/28/2004	One time programmable memory	TANG, STEPHEN H.
<a href="#">11038134</a>	Not Issued	41	01/21/2005	Bias generator for body bias	TANG, STEPHEN H.
<a href="#">11038394</a>	Not Issued	71	01/21/2005	Bias generator for body bias	TANG, STEPHEN H.
<a href="#">11053786</a>	Not Issued	30	02/09/2005	Non strobe sensing circuit	TANG, STEPHEN H.
<a href="#">11134450</a>	Not Issued	30	05/23/2005	Reducing power consumption in integrated circuits	TANG, STEPHEN H.
<a href="#">11151982</a>	Not Issued	30	06/14/2005	Purge-based floating body memory	TANG, STEPHEN H.
<a href="#">11158518</a>	Not Issued	30	06/21/2005	Apparatus and method for programming a memory array	TANG, STEPHEN H.
<a href="#">11170504</a>	Not Issued	30	06/29/2005	Capacitor structure for a logic process	TANG, STEPHEN H.
<a href="#">11239903</a>	Not Issued	30	09/30/2005	Dual gate oxide one time programmable (OTP) antifuse cell	TANG, STEPHEN H.
<a href="#">11268098</a>	Not Issued	30	11/07/2005	Asymmetric memory cell	TANG, STEPHEN H.

<a href="#">11268430</a>	Not Issued	30	11/07/2005	Memory cell without halo implant	TANG, STEPHEN H.
<a href="#">11289621</a>	<a href="#">7057927</a>	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
<a href="#">11295400</a>	Not Issued	30	12/06/2005	Component reliability budgeting system	TANG, STEPHEN H.
<a href="#">11320789</a>	Not Issued	30	12/30/2005	Method and apparatus to clamp SRAM supply voltage	TANG, STEPHEN H.

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